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09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

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SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 PENNSYLVANIA AVE. N.W.
WASHINGTON,, DC 200373202

EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	PAPER NUMBER
2123	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2007 and 02 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on May 2, 2007 and Appeal Brief filed on October 2, 2007. Claims 2-4 of the application were amended. Claims 1-4 of the application are pending. This office action is made non-final.

Prosecution reopened

2. In view of the Appeal Brief filed on October 2, 2007, PROSECUTION IS HEREBY REOPENED as set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

PAUL RODRIGUEZ
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Claim Rejections - 35 USC § 101

3. Claims 1 and 2 are rejected under 35 U.S.C. 101, as reciting nonfunctional descriptive material. See MPEP Section 2106(II)(A) and 2106(IV)(B)(1).

3.1 Regarding Claim 1, it is directed to a delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits, and for at least one circuit of said plurality of circuits, said library further comprises logical operation information. Therefore, the system comprises a library of data. Therefore, the claim describes non functional descriptive material which is non statutory subject matter. Merely claiming nonfunctional descriptive material stored in a computer library does not make the invention eligible for patenting.

3.2 Regarding Claim 1, it is directed to a delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits, and for each of said plurality of circuits,

said library further comprises logical operation information. Therefore, the system comprises a library of data. Therefore, the claim describes non functional descriptive material which is non statutory subject matter. Merely claiming nonfunctional descriptive material stored in a computer library does not make the invention eligible for patenting.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hasegawa** (U.S. Patent 6,041,168) in view of **Hasegawa** (U.S. Patent 5,528,511).

6.1 **Hasegawa** '168 teaches high-speed delay verification apparatus and method therefor. Specifically, as per Claim 1, **Hasegawa** '168 teaches the delay analysis system for making a delay analysis of a logic circuit (CL1, L5-8);

the system having a delay analysis library comprising connection information and delay time information for a plurality of circuits wherein, for at least one circuit of said plurality of circuits, said library further comprises logical operation information (CL1, L58-61 and CL2, L30-35).

Hasegawa '168 does not expressly teach that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output

terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; CL2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; CL3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Hasegawa** '168 with the system of **Hasegawa** '511 that included delay time information provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information was specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay time information for each signal path of the logical circuit of the at least one circuit was based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information, because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process (CL2, L61-65).

6.2 As per Claim 2, **Hasegawa** '168 teaches the delay analysis system for making a delay analysis of a logic circuit (CL1, L5-8);

the system having a delay analysis library comprising connection information and delay time information for a plurality of circuits wherein, for each of said plurality of circuits, said library further comprises logical operation information (CL1, L58-61 and CL2, L30-35).

Hasegawa '168 does not expressly teach that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein the delay time information for each signal path of the logical circuit of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the plurality of circuits. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals to output terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein the delay time information for each signal path of the logical circuit of the plurality of circuits is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the plurality of circuits (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; CL2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of

the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; CL3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

6.3 As per Claim 3, **Hasegawa** '168 teaches a method of making delay analysis of a logical circuit (CL1, L5-8); comprising:

referencing a delay analysis library for a plurality of circuits, the delay analysis library comprising connection information, delay time information and logic operation information (CL1, L58-61 and CL2, L30-35).

Hasegawa '168 does not expressly teach that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting

logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; C2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; C3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Hasegawa '168 does not expressly teach if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low

state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; CL2, L30-42; CL3, L5-26).

6.4 As per Claim 4, **Hasegawa** '168 teaches a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, the computer-readable medium causing a computer to execute the method (CL1, L5-8); wherein the method comprises:

referencing a delay analysis library for a plurality of circuits, the delay analysis library comprising connection information, delay time information and logic operation information (CL1, L58-61 and CL2, L30-35).

Hasegawa '168 does not expressly teach that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output

terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay time information is provided for a signal path from input terminals of a logical circuit and wherein delay time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay time information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at each output terminal as represented by logical operation information for the at least one circuit (Fig. 3; CL1, L28-35; CL2, L30-42; CL3, L5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; CL1, L28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; C2, L30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; C3, L5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Hasegawa '168 does not expressly teach if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting a delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; CL2, L30-42; CL3, L5-26).

Hasegawa '168 does not expressly teach performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit. **Hasegawa** '511 teaches performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit (CL3, L5-26).

Response to Amendments

7. Applicants' arguments, filed on May 2, 2007 and the Appeal Brief of October 2, 2007 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

Argument in Amendment of May 2, 2007

7.1 As per the applicants' argument that "in the claimed invention, the delay time is determined by comparing the input signal at a first point and the propagated signal (signal at a subsequent circuit point after propagation) at the second point; if the data signal of a first flip-flop is "rising edge" at the first time point when a clock signal is input, then, at the time point when the next clock signal is received, the question is whether or not the propagated signal at the next flip-flop is propagated as "rising edge" (in other words, whether the next trigger of the clock signal can occur in association with the rising edge of the propagated signal); Figure 3, for example, represents the logical consequence of an AND gate (two inputs 1 and 2, and output 3) of figure 2; assume the case where the state changes LOW-HIGH-LOW within a period of two clock signals; at the time in which the second clock signal is input, the state is "LOW," which is regarded to be the same state as the first signal state; thus, there is no recognition of "rising" (LOW-HIGH) in view of the operation per clock unit; therefore, the case where the delay is "NONE" (at the column Rise/Fall), will not indicate any change in the signal state (between

LOW and HIGH) which means that there is no need to make a target (object) of the timing analysis for the case "NONE" in figure 3. in the claimed invention, the situation where there is no change in signal state (i.e., a nullified state) is determined automatically as a result of the logic AND circuit; on the other hand, in Hasegawa '511, the occurrence of a "nullified state" must be identified explicitly. ", the Examiner takes the position that how the implementation is done differently does not affect what is claimed in the claims. The Examiner has shown that prior art teaches the claimed invention.

Arguments in the Appeal Brief of October 2, 2007

7.2 As per the applicants' argument that "Hasegawa `511 fails to teach a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal as taught by the subject application; Blinne et al., Hasegawa `168 and Hasegawa `511 fail to teach or suggest, either alone or in combination, a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal", the examiner respectfully disagrees.

Hasegawa '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa** '511 discusses at CL1, L28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa** '511 states at CL2, L30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical

operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa** '511 describes at CL3, L5-26 that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified. Therefore, **Hasegawa** '511 teaches a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (CL2, L61-65).

7.3 As per the applicants' argument that "Hasegawa `511 teaches a delay time verifying, wherein the rise and fall are not permitted between nodes connected by a short circuit (Col 3, L3-26); Hasegawa `511 confusingly teaches an OR gate which fails to respond to two simultaneously hi inputs (Fig.3); Hasegawa `511 teaches that input and output paths in a given OR gate are equal with respect to delay; ...", the Examiner respectfully disagrees.

The Examiner takes the position that Hasegawa `511 does not teach at Col 3, L3-26, a delay time verifying, wherein the rise and fall are not permitted between nodes connected by a short circuit; Hasegawa `511 does not confusingly or otherwise teach at Fig.3, an OR gate which fails to respond to two simultaneously hi inputs. Hasegawa `511 does not teach that input and output paths in a given OR gate are equal with respect to delay.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
November 15, 2007